

**Patent**

Customer No. 31561  
Docket No. 10547-US-PA  
Application No.: 10/710,020

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**  
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In re application of

Applicant : Huang et al.  
Application No. : 10/710,020  
Filed : June 14, 2004  
For : PROCESS FOR FABRICATING BUMPS  
Examiner : VAN, LUAN V  
Art Unit : 1753

**JUL 2 - 2007**

**TRANSMITTAL LETTER**  
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In response to the Notice of Appeal filed on May 14, 2007, please find the relevant paper as follows:

- Appeal Brief in (14) pages.

Please charge the payment in the amount of US\$500 to Account No. 50-2620 (Order No.: 10547-US-PA) to cover the fee set forth in 37 CFR 1.17(c) for filing the Appeal Brief.

Thank you for your attention and assistance in the subject matter. If you have any questions, please feel free to contact the undersigned.

Respectfully Submitted,  
JIANQ CHYUN Intellectual Property Office

Date: July 1, 2007

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PATENT

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE  
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

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EX PARTE HUANG ET AL.

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Application for Patent

Filed June 14<sup>th</sup>, 2004

Serial No. 10/710,020

FOR:

PROCESS FOR FABRICATING BUMPS

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APPEAL BRIEF

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USSN 10/710,020

USSN 10/710,020

Appeal Brief

## TABLE OF CONTENTS

	<u>Page No.</u>
I. Real party in interest .....	1
II. Related appeals and interferences .....	1
III. Status of the claims .....	1
IV. Status of amendments .....	1
V. Summary of claimed subject matter .....	1
VI. Grounds of rejection to be reviewed on appeal .....	2
<i>Were claims 1-10 properly rejected under 35 U.S.C. 103(a) as being obvious over Bojkov et al. (U.S. 2004/0140219; hereafter Bojkov) in view of Chung et al. (U.S. 6,409,903; hereafter Chung) and Jao (U.S. 6,415,974; hereafter Jao)?</i> .....	
	2
<i>Were claim 11 properly rejected under 35 U.S.C. 103(a) as being obvious over Bojkov in view of Chung, Jao and Ihara et al. (U.S. 6,030,512; hereafter Ihara)?</i> .....	
	2
VII. Arguments .....	2
A. The related law .....	2
B. Grouping of the claims .....	3
C. <i>Claims 1-10 were improperly rejected under 35 U.S.C. 103(a) as being obvious over Bojkov in view of Chung and Jao.</i> .....	4
D. <i>Claim 11 were improperly rejected under 35 U.S.C. 103(a) as being obvious over Bojkov in view of Chung, Jao and Ihara et al. (U.S. 6,030,512; hereafter Ihara).</i> ..	7
E. Conclusion. ....	8
VIII. Claims appendix .....	10
IX. Evidence appendix .....	12
X. Related proceedings appendix .....	12

USSN 10/710,020

Appeal Brief

**I. Real party in interest**

The real party in interest is ADVANCED SEMICONDUCTOR ENGINEERING, Inc., the assignee of record.

**II. Related appeals and interferences**

There are no related appeals and/or interferences.

**III. Status of the claims**

A total of 11 claims were presented during prosecution of this application. Appellants appeal rejected claims 1-11.

**IV. Status of amendments**

A proposed amendment was filed by appellants on November 29<sup>th</sup>, 2006, proposing amendments to the claims by adding claim 11-18 in response to the first Office Action dated on August 29<sup>th</sup>, 2006. In the Final Office Action dated January 18<sup>th</sup>, 2007, the proposed amendment filed on November 29<sup>th</sup>, 2006 was entered. In response to the Final Office Action, the appellants filed a response on April 4<sup>th</sup>, 2007 without further amendment.

**V. Summary of claimed subject matter**

The claimed subject matter of the present invention involved in the appeal is directed to a process for fabricating bumps with different size and height. In order to fabricate bumps with different size and height, as shown in Fig. 2 and paragraph [0023] of the present invention, a photoresist layer is formed over a wafer having a plurality of bonding pads and passivation layer thereon (step S2). Additionally, the passivation layer is disposed on a surface of the wafer and exposes the bonding pads and the photoresist layer has a plurality of openings with different widths and the openings are positioned corresponding to the bonding

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USSN 10/710,020

Appeal Brief

pads. Since the openings in the photoresist layer have different width, it is necessary to control the diffusion of the metallic ion in the electrolytic solution to successfully diffuse into the narrow openings in the photoresist layer. In the present invention, a novel control mechanism is introduced. By applying an increasing step current to an electrolytic solution, the metallic ions within the electrolytic solution has enough time to diffuse into the narrow openings (Figs. 3A and 3B and paragraph [0029]). Therefore, the electroplating rate inside openings of variant widths is constant and the thickness of the bump inside each opening is uniform. Furthermore, in the present invention, each step of the increasing step current can be composed of several current pulses (as shown in Fig. 4A, Fig. 4B and Fig. 4C). In the plating control mode of the increasing step current with current pulses, by applying the reverse pulse current during the electroplating cycle, some of the conductive material adhered to the mouth regions of the openings can be electrolyzed (paragraph [0030]). Hence, the problem of blocking the mouth of the openings during filling the openings and the formation of voids inside the bump can be solved. Therefore, the height of the bumps can be well controlled after a reflow process.

#### VI. Grounds of rejection to be reviewed on appeal

*Were claims 1-10 properly rejected under 35 U.S.C. 103(a) as being obvious over Bojkov et al. (U.S. 2004/0140219; hereafter Bojkov) in view of Chung et al. (U.S. 6,409,903; hereafter Chung) and Jao (U.S. 6,415,974; hereafter Jao)?*

*Were claim 11 properly rejected under 35 U.S.C. 103(a) as being obvious over Bojkov in view of Chung, Jao and Ihara et al. (U.S. 6,030,512; hereafter Ihara)?*

#### VII. Arguments

##### A. The related law

“To prevent the use of hindsight base on the invention to defeat patentability of the invention, this court requires the examiner to show a motivation to combine the references that create the case of obviousness. In other words, the examiner must show reasons that the

USSN 10/710,020

Appeal Brief

skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed." *In re Rouffet*, 149 F.3d 1350, 47 USPQ2d 1453 (Fed. Cir. 1998).

When more than one reference or source of prior art is required in establishing the obviousness rejection, "it is necessary to ascertain whether the prior art teachings would appear to be sufficient to one of ordinary skill in the art to suggest making the claimed substitution or other modification." *In re Lalu*, 747 F.2d 703, 223 USPQ 1257, 1258 (Fed. Cir. 1984). There must be some motivation to combine the references; this motivation must come from "the nature of the problem to be solved, the teachings of the prior art, [or] the knowledge of persons of ordinary skill in the art." *In re Rouffet*, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457-58 (Fed. Cir. 1998). "Particular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed." *In re Kozab*, 217 F.3d 1365, 1371 (Fed. Cir. 2000).

Most if not all inventions arise from a combination of old elements....Thus, every element of a claimed invention may often be found in the prior art....However, identification in the prior art of each individual part claimed is insufficient to defeat patentability of the whole claimed invention. *In re Kotzab*, 217 F.3d 1365, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000).

If a reference would be "rendered inoperable for its intended purpose" when it is modified for use as prior art, then the reference "teaches away" and should not be used. *In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1125, 1127 (Fed. Cir. 1984).

#### B. Grouping of the claims

For the ground of rejection contested by appellants in this appeal, claims 1-11 may be treated as one group to stand or fall together. Independent claim 1, the sole independent claim pending, may be taken as representatives for the issue on appeal.

USSN 10/710,020

Appeal Brief

C. *Claims 1-10 were improperly rejected under 35 U.S.C. 103(a) as being obvious over Bojkov in view of Chung and Jao.*

1. The rejection

The Final Office Action, dated January 18<sup>th</sup>, 2007, rejected claims 1-10 under 35 USC §103(a) over Bojkov et al. (U.S. 2004/0140219; hereafter Bojkov) in view of Chung et al. (U.S. 6,409,903; hereafter Chung) and Jao (U.S. 6,415,974; hereafter Jao). In making the rejection, the Examiner has construed Bojkov to disclose the process for fabricating bumps except openings having different width and the increasing of the current. The Examiner cites Chung to teach a current applied to the anode and cathode substrate, wherein the current is preprogrammed to ramp up to a current value from a first current value. The Examiner further cites Jao to teach a method for forming bumps having a plurality of openings with various sizes.

2. The prior art

Bojkov discloses a method for current pulse plating in the integrated device. As shown in Figs. 2A to 2D and paragraph [0015] and paragraph [0032] of Bojkov's application, the stud 32 and the bump 34 can be formed using plating processes that include applying the conductive materials forming the stud 32 and the bumps 34 using pulse plating. The pulse plating includes interrupting the application of current from current source 24 (Fig. 1) with relaxation periods such that the application of current is periodic during the plating process.

Chung discloses a multi-step potentiostatic/galvanostatic plating control. In Fig. 3, Fig. 4 and col. 3, lines 49-54 and col. 7, lines 14-17 of Chung's application, Chung shows that the seed layer on the wafer used to initiate plating suffers from being burn-through at the contact point and Chung further introduce the procedure of ramping the current from a low value to a high value to avoid the phenomenon of the burn-through of the seed layer of the wafer.

Jao discloses the different opening width. However, Jao has proposed the different mechanism by adjusting the area of the UBM 204 (col. 4, lines 31-32; FIG. 2A). Jao further emphasizes that "To improve the coplanarity of the solder bumps structure either using the various sizes of openings of the UBM layer to control the solder volume or using the various



USSN 10/710,020

Appeal Brief

UBM structures to control the height of the solder bumps, or using a combination thereof" (col. 5 lines 43-47).

3. The prior art differentiated

The proposed invention is directed to provide a process for fabricating bumps to solve the problem due to the openings with different widths. Since the electroplating operation is taken, the openings with different widths may cause the problem as discussed in specification at paragraphs [0008]-[0009]. That is, when the opening for forming the bump is too narrow or too deep, mass transfer of the electrolytic solution is usually poor. Hence, the metallic ions within the electrolytic solution can hardly diffuse into the openings. Particularly, when the aspect ratio is greater than 1.2, the problem does apparently exist. By applying an increasing step current, as for example shown in FIGs. 3A-3B and FIGs. 4A-4C, the metallic ions within the electrolytic solutions has enough time to diffuse into the narrow openings in the photoresist layer. Thus, the electroplating rate inside the openings of variant widths is constant and the thickness of the bump inside each opening is uniform.

As clearly shown in the prior art Bojkov and admitted by the Examiner, the electrical current 120 and 122 are in two levels by alternating change while the relaxation period 124 is between adjacent two step currents ([0040]). Apparently, Bojkov fails to disclose the increasing step current for the opening with different width. Furthermore, also shown in paragraph [0040], Bojkov emphasizes that "Each cathodic current 120 and anodic current 122 is followed by a relaxation period 124". That is, the relaxation period is an essential element of Bojkov's application.

The Office Action cites Chung for teaching that, as shown in Fig. 4 of Chung's application, the particular current is used with is preprogrammed to ramp up to a constant current value from a first current value I(1) to I(4). However, Chung clearly shows that the reason for ramping up the current to a constant current value without exceeding the threshold voltage is to prevent the seed layer on the wafer from being burn-through (as shown in col. 7, lines 14-17 and lines 46-56).

The Office Action also cites Jao for teaching that the bumps are formed within a plurality of openings with various sizes. However, Jao clearly mentions that "To improve the coplanarity of the solder bumps structure either using the various sizes of openings of the



USSN 10/710,020

Appeal Brief

UBM layer to control the solder volume or using the various UBM structures to control the height of the solder bumps, or using a combination thereof" (col. 5 lines 43-47).

None of Bojkov and Chung raises the issue of forming the bumps by using the photoresist layer having a plurality of openings with different widths. Neither Bojkov nor Chung considers the narrow openings in the photoresist layer would lead to a poor mass transfer of the electrolytic solution and cause non-uniform thicknesses of the bumps. Although Jao points out an issue similar to what has been discussed in the present invention, Jao also provides a way to solve the problem. That is, Jao states that by either using the various sizes of openings of the UBM layer to control the solder volume or using the various UBM structures to control the height of the solder bumps, or using a combination thereof, the coplanarity of the solder bump structure can be improved. On the other words, Jao's application is complete itself. Therefore, people skilled in the art who suffer from non-uniform thickness bumps might not think to modify Bojkov in view of Chung and Jao as Jao already provides the skill artisan another way to solve the problem.

4. Even if combined Bojkov, Chung and Jao

The Office Action combines Bojkov with Chung and Jao to modify the pulse plating current disclosed by Bojkov to include the ramping current taught by Chung and the various sizes of openings of the UBM layer taught by Jao. However, even if combined Bojkov with Chung and Jao, the combination result would jeopardize Bojkov's application. That is, as mentioned above, Bojkov emphasizes the relaxation period should follow each cathodic current and anodic current 122 is followed by a relaxation period 124. More specifically, for each current level, a relaxation period is insisted to follow the end of the current level. The relaxation period is an essential feature of Bojkov's application. Even though Chung provides a concept for using a ramping current for plating, replacing the ramping current would ruin the main inventive concept of Bojkov. Further, even though people skilled in the art did modify Bojkov in view of Chung and Jao and keep Bojkov's essential feature, the current curve of the combination result is still different from that of the proposed invention.

USSN 10/710,020

Appeal Brief

D. *Claim 11 were improperly rejected under 35 U.S.C. 103(a) as being obvious over Bojkov in view of Chung, Jao and Ihara et al. (U.S. 6,030,512; hereafter Ihara).*

1. The rejection

The Final Office Action, dated January 18<sup>th</sup>, 2007, rejected claim 11 under 35 USC §103(a) over Bojkov et al. (U.S. 2004/0140219; hereafter Bojkov) in view of Chung et al. (U.S. 6,409,903; hereafter Chung), Jao (U.S. 6,415,974; hereafter Jao) and Ihara et al. (U.S. 6,030,512; hereafter Ihara). In making the rejection, the Examiner has construed Bojkov in view of Chung and Jao the proposed invention except the limitation of the aspect ratio. The Examiner cites that Ihara teaches the aspect ratio of a bump to be formed can be a value not over than 0.5.

2. The prior art

As discussed above, there is no motivation for the skill artisan to combine Bojkov with Chung and Jao since none of Bojkov and Chung confronts the problem which the proposed invention faces. In addition, even though Jao mentions about the problem about uneven solder bump structure, Jao also provides a way, which is nothing to do with the current control, to solve the problem. Even if people skilled in the art did combine Bojkov with Chung and Jao in a way as Examiner thought, the combination not only ruin Bojkov's main inventive feature in order to fit the proposed invention but also lack of the requirement of the aspect ratio.

Ihara teaches the method for forming bumps and mentions that the thickness of the resist layer and the diameter of the fine hole are adjusted so that the aspect ratio of the bump to be formed can be a value not lower than 0.5.

3. The prior art differentiated

As discussed above, proposed invention is directed to a process for fabricating bumps to solve the problem due to the openings with different widths. Since the electroplating operation is taken, the openings with different widths may cause the problem as discussed in specification at paragraphs [0008]-[0009]. That is, when the opening for forming the bump is too narrow or too deep, mass transfer of the electrolytic solution is usually poor. Hence, the metallic ions within the electrolytic solution can hardly diffuse into

USSN 10/710,020

Appeal Brief

the openings. Particularly, when the aspect ratio is greater than 1.2, the problem does apparently exist. By applying an increasing step current, as for example shown in FIGs. 3A-3B and FIGs. 4A-4C, the metallic ions within the electrolytic solutions has enough time to diffuse into the narrow openings in the photoresist layer. Thus, the electroplating rate inside the openings of variant widths is constant and the thickness of the bump inside each opening is uniform.

However, none of the cited arts including Bojkov, Chung and Ihara suggests or teaches formation of the bumps by using a photoresist layer with a plurality of openings with different widths. None of the aforementioned citations mentions that the openings having different widths in the photoresist layer for forming bumps would lead to poor mass transfer of the electrolytic solution and cause non-uniform thickness of the bumps. Although Jao does mention about the problem about uneven solder bump structure, Jao, himself, also provides a way, which is nothing to do with the current control, to solve the problem.

4. Even if combined Bojkov, Chung, Pao and Ihara

As discussed above, the combination of Bojkov, Chung, Jao and Ihara still fails to render the proposed invention unpatentable. Even though Chung provides a concept for using a ramping current for plating, replacing the ramping current would ruin the main inventive concept of Bojkov. Further, even though people skilled in the art did modify Bojkov in view of Chung, Jao and Ihara and keep Bojkov's essential feature, the current curve of the combination result is still different from that of the proposed invention. Therefore, Appellants respectfully submit to the Board that the teachings of Bojkov, Chung, Jao and Ihara are deficient in rendering claim 11 unpatentable.

E. Conclusion.

As noted, none of the cited art, either alone or in combination, can be said to render obvious the appealed claims. None of the reference Bojkov and Chung teaches the use of photoresist layer having openings with different widths for forming the bumps. People skilled in the art who suffer from non-uniform thickness bumps might not think to modify

USSN 10/710,020

Appeal Brief

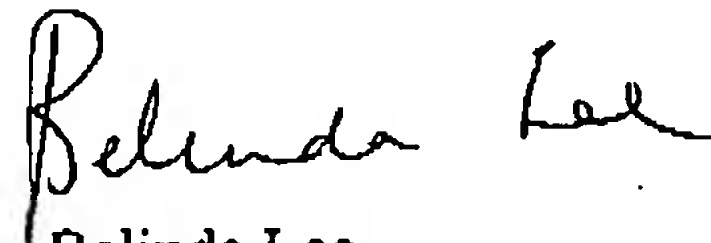
Bojkov in view of Chung and Jao as Jao already provides the skill artisan another way to solve the problem.

Accordingly, Appellants believe that the rejections under 35 U.S.C. §103 are in error, and respectfully requests the Board of Patent Appeals and Interferences to reverse the Examiner's rejections of the claims on appeal.

Date :

*July 2, 2007*

Respectfully submitted,



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USSN 10/710,020

Appeal Brief

## VIII. Claims appendix

CLAIMS ON APPEAL:

Claim1 (original) A process for fabricating bumps, comprising the steps of:  
providing a wafer having a plurality of bonding pads and a passivation layer thereon, wherein the passivation layer is disposed on a surface of the wafer and exposes the bonding pads;  
forming a photoresist layer over the wafer, wherein the photoresist layer has a plurality of openings with different widths and the openings are positioned corresponding to the bonding pads; immersing the wafer into an electrolytic solution; and performing an electroplating operation by providing an increasing step current to the electrolytic solution.

Claim2 (original) The bump fabrication process of claim 1, wherein the increasing step current is set between  $I_{min}$  and  $I_{max}$ , wherein  $I_{min}$  is a smallest current to start the electroplating operation and  $I_{max}$  is a largest permissible current for performing the electroplating operation.

Claim3 (original) The bump fabrication process of claim 1, wherein the step current comprises a plurality of linear currents.

Claim4 (original) The bump fabrication process of claim 3, wherein the step of performing an electroplating operation further comprises stopping providing the step current for a brief period, so that the electroplating operation is temporarily suspended.

Claim5 (original) The bump fabrication process of claim 1, wherein the step current comprises a plurality of pulse currents, each having a peak current and a trough current.

USSN 10/710,020

Appeal Brief

Claim6 (original) The bump fabrication process of claim 5, wherein the peak current is set between  $I_{min}$  and  $I_{max}$ .

Claim7 (original) The bump fabrication process of claim 5, wherein the trough current is selected from the group consisting of a positive current smaller than  $I_{min}$ , a zero current and a negative current.

Claim8 (original) The bump fabrication process of claim 1, wherein the step current comprises at least a pulse current and a plurality of linear currents and the pulse current comprises a peak current and a trough current.

Claim9 (original) The bump fabrication process of claim 8, wherein the peak current is set between  $I_{min}$  and  $I_{max}$ .

Claim10 (original) The bump fabrication process of claim 8, wherein the trough current is selected from the group consisting of a positive current smaller than  $I_{min}$ , a zero current and a negative current.

Claim11 (previously presented) The bump fabrication process of claim 1, wherein at least one of the openings has an aspect ratio of greater than 1.2.

**PATENT****IX. Evidence appendix**

There is no evidence submitted pursuant to §§ 1.130, 1.131, or 1.132 of this title or of any other evidence entered by the examiner and relied upon by appellant in the appeal, along with a statement setting forth where in the record that evidence was entered in the record by the examiner.

**X. Related proceedings appendix**

There are no decisions rendered by a court or the Board in the proceeding identified in the Related Appeals and Interferences section of the brief.